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SPECIFICATION

1. Title of the Invention

Method of Manufacturing Semiconductor Integrated Circuit

2. Scope of Claim for Patent

1) A method of manufacturing a semiconductor integrated circuit including a MISFET which consists of a low impurity concentration region in which source and drain diffusion layer regions are closed to a channel forming region and a high impurity concentration region other than the above region, characterized in that when said low impurity concentration diffusion layer region and said high impurity

concentration diffusion layer region are formed, the thickness of a gate insulating film on a region where said low impurity concentration diffusion layer is formed is thicker than that of a gate insulating film on a region where said high impurity concentration diffusion layer is formed and an ion implantation is executed by using those gate insulating films and a gate electrode as masks.

3. Detailed Description of the Invention

[Industrial use of the Invention]

The present invention relates to a method of manufacturing a semiconductor integrated circuit including an MIS field effect transistor (FET) which consists of a low impurity concentration region in which source and drain diffusion layer regions are closed to a channel forming region and a high impurity concentration region other than the above region.

[Prior Art]

In order to realize a high voltage withstanding of a MISFET, at the present time, there is widely used a structure in which on end portions of source and drain diffusion layer regions on the side of a channel forming region, diffusion layer regions having the same conductivity type and a relatively low impurity concentration are provided. Figs. 2(a) to (e) show a method of introducing impurities into a source region and a drain region in the

method of manufacturing a MOSFET having such a structure. First, an ion implantation of phosphorus 4 of a low dose such as about 1 x $10^{13}/cm^2$ is performed by using a polysilicon gate electrode 3 formed on a P type silicon substrate 1 through a gate oxide film 2 as a mask (Fig. 2(a)). After the gate electrode 3 and a region to be set as a low impurity concentration region in the source and drain diffusion layers are covered by a photo resist film 5 (Fig. 2(b)), the ion implantation of phosphorus of a high dose such as about 5 x $10^{15}/cm^2$ is again executed (Fig. 2(c)). After the photo resist film 5 is removed (Fig. 2(d)), a heat treatment is performed, thereby forming the source and drain diffusion layer regions of the MOSFET having a high voltage withstanding structure having N type diffusion regions 6 and 7 of a low impurity concentration and a high impurity concentration (Fig. 2(e)). When the MOSFET including the source and drain low impurity concentration diffusion layers 6 formed by the above-mentioned processes is used, an electric field concentration in the drain diffusion layer is relieved as compared with that of the normal MOSFET, so that a voltage withstanding between the source and the drain is improved.

In the recent semiconductor integrated circuit device, a technique to integrate the MISFET which intends to realize a high voltage withstanding as mentioned above and a fine

MISFET which intends to realize a high processing speed and a high integration onto the same substrate is important. In case of integrating the FET which intends to realize the high processing speed and high integration and the FET which intends to realize the high voltage withstanding on the same substrate, it is necessary to conquer the following problem point. That is, in the FET which intends to realize the high processing speed and high integration, it is necessary to relatively thin the thickness of gate insulating film and, in the FET which intends to realize the high voltage withstanding, it is necessary to relatively thick on the thickness. In the conventional semiconductor device, however, since the above-mentioned two kinds of FETs are formed on the same gate dielectric film, it is very difficult to simultaneously satisfy the realization of high processing speed and high integration and the realization of high voltage withstanding. As means for conquering the problem point, the semiconductor device having a structure in which a gate dielectric film having two kinds or more of film thicknesses is provided on the same substrate has been disclosed in Japanese Patent Application No. 63-201473 according to the patent application by the same applicant as the present invention. Figs. 3(a) to (d) show an example of a process for forming a gate oxide film in the above-mentioned semiconductor device. The process will now be

explained hereinbelow. First, a field oxide film 8 is formed on the P type Si substrate 1 except for a device region by a normal selective oxidation method and, after that, the oxide film remained on the device region is eliminated (Fig. 3(a)). By a heat treatment in dry oxygen, the gate oxide film 2 of 1800 Å is formed on the whole surface of a wafer including the device region (Fig. 3(b)). After a portion except for the device region, in which a high voltage withstanding N channel MOSFET is formed, is covered by the photo resist film 5, the gate oxide film 2 in the portion of the above-mentioned device region is removed by a wet etching by hydrofluoric acid (Fig. 3(c)). Subsequently, the photo resist film 5 is eliminated by a resist ashing using O_2 plasma and, after that, the gate oxide film having a thickness of 400 Å is formed on the whole surface of the wafer including the device region by the heat treatment in dry oxygen. By the above-mentioned process, a gate oxide film 21 having a thickness of 2000 Å can be formed on the device region of the N type FET of a high voltage withstanding and a gate oxide film 22 having a thickness of 400 Å can be formed on the device region of the N type FET of a high integration and a high processing speed (Fig. 3(d)).

[Problems sought to be Solved by the Invention]

Each of the manufacturing methods shown in Figs. 2 and 3 is a manufacturing method suitable for forming the MISFET which intends to realize the high voltage withstanding and the MISFET which intends to realize the high processing speed and the high integration on the same substrate. By combining both of the manufacturing methods, the high voltage withstanding MISFET and the high processing speed and high integration MISFET can be formed on the same substrate and, further, the thickness of gate insulating film can be thicken in the high voltage withstanding FET and it can be thinned in the high processing speed and high integration FET. In case of simply combining those manufacturing methods, however, the number of processes added in correspondence to those objects is obtained by simply adding, so that there is such a problem that the number of processes remarkably increases as compared with that of the manufacturing procedure of the conventional standard MISFET.

It is an object of the present invention to provide a method of manufacturing a semiconductor integrated circuit in which even when a high voltage withstanding MISFET is integrated together with the different kind of MISFET on the same semiconductor substrate, the number of processes is small.

[Means of Solving the Problems]

In order to accomplish the above object, there is provided a method of manufacturing a semiconductor integrated circuit including a MISFET which consists of a low impurity concentration region where source and drain diffusion layer regions are closed to a channel forming region and a high impurity concentration region other than the above region, wherein when the low impurity concentration diffusion layer region and the high impurity concentration diffusion layer region are formed, the thickness of a gate insulating film on a region where the low impurity concentration diffusion layer is formed is thicker than that of a gate insulating film on a region where the high impurity concentration diffusion layer is formed and an ion implantation is executed by using those gate insulating films and a gate electrode as masks.

[Operation]

By doping impurities into a region having different gate insulating films due to an ion implantation, diffusion layer regions having two kinds of impurity concentrations can be formed by the ion implantation of only once. Consequently, the low impurity concentration region and the high impurity concentration region in the source and drain diffusion layers of the MISFET which intends to realize a high voltage withstanding can be formed together with the source and drain diffusion layers of the MISFET which

intends to, for example, realize a high processing speed and a high integration on the same semiconductor substrate by the same processes, so that the number of processes can be reduced.

[Embodiment]

Figs. 1(a) to (e) show manufacturing processes in an embodiment of the present invention with respect to a portion of a high voltage withstanding MOSFET shown on the left of each diagram and a portion of a MOSFET of a high processing speed and a high integration on the same substrate shown on the right of each diagram, respectively. The same reference numerals are applied to portions common to those in Figs. 2 and 3. In a manner similar to the method shown in Fig. 3, the gate oxide film 2 of 1800 Å is formed on the whole surface on the P type Si substrate (Fig. 1(a)). By the selective etching and the heat treatment in dry oxide to the oxide film, the gate oxide films 21 and 22 of two kinds of film thicknesses are formed (Fig. 1(b)). In this instance, in the high voltage withstanding MOSFET, the thickness of gate oxide film 22 on the region where the low impurity concentration diffusion layer is formed is set to 2000 Å and the thickness of gate oxide film 21 on the region where the high impurity concentration diffusion layer is formed is set to 400 Å. In the high processing speed and high integration MOSFET, the gate oxide film 21 having the

film thickness of 400 Å is formed. The gate electrode 3 is made of polysilicon (Fig. 1(c)) and, after that, the ion implantation of phosphorus 4 is executed in a self-aligning manner by using the gate electrode 3 as a mask (Fig. 1(d)). As ion implanting conditions at that time, P_{31}·ion is used, an acceleration voltage is set to 90 keV, and a dose is set to $3.5 \times 10^{15}/cm^2$. In this instance, a dose of P_{31}·ion 4 which reaches the P type silicon substrate depends on the thickness of gate oxide film on the surface of the substrate. As the thickness of gate oxide film is thicker, the dose of P_{31}·ion which reaches the silicon substrate is smaller. Therefore, when a heat treatment is executed in a nitrogen atmosphere, P_{31}·ion is diffused and activated, and the N type diffusion layer is formed (Fig. 1(e)), the diffusion layer under the gate oxide film 22 having a film thickness of 2000 Å becomes the source and drain regions 6 in the N type low impurity concentration diffusion layer and the diffusion layer under the gate oxide film 21 having a film thickness of 400 Å becomes the source and drain regions 7 in the N type high impurity concentration diffusion layer. Concentration distributions of the above diffusion layers are shown in Figs. 4 and 5. Fig. 4 shows the concentration distribution of the N type high impurity concentration diffusion layer 7. Fig. 5 shows the concentration

distribution of the N type low impurity concentration diffusion layer 6. In both of the graphs, a line 11 denotes an N type concentration distribution and a line 12 indicates a P type concentration distribution. As will be understood from the graphs, the N type high impurity concentration diffusion layer 7 has a concentration distribution suitable for driving the FET of the high processing speed and high integration. The N type low impurity concentration diffusion layer 6 has an enough concentration distribution for relieving the electric field concentration in the drain portion in the high voltage withstanding FET.

According to the above-mentioned method, the manufacturing processes according to the conventional method shown in Fig. 3 in which the gate oxide film having the two kinds of film thicknesses is formed on the same substrate are not changed at all, only the thickness of gate oxide film of the source and drain portions in the high voltage withstanding MOSFET of a pattern to separate the film thickness into two kinds of thicknesses by an etching is changed, so that the high voltage withstanding FET as shown in Fig. 2 can be formed together with the FET of the high processing speed and high integration on the same substrate. That is, as compared with the case where the conventional methods in Figs. 2 and 3 are combined, the processes of Figs. 2(a) and (b) in the forming processes of the low

impurity concentration diffusion layer shown in Figs. 2 can be omitted.

[Effects of the Invention]

According to the invention, by using the processes on the basis of the method in which the gate insulating films having the different thicknesses for the high voltage withstanding MISFET and the high processing speed and high integration MISFET are formed on the same substrate and which has already been filed, the pattern to separate the film thickness of gate insulating film in the source and drain portions of the high voltage withstanding MOSFET into two kinds of thicknesses is merely prepared, so that the source and drain portions of the high voltage withstanding MISFET and, for example, the MISFET of the high processing speed and the high integration can be simultaneously formed by the ion implanting process of once. Therefore, it is extremely effective in reducing the number of processes at the time of the manufacturing of the semiconductor integrated circuit including the high voltage withstanding MISFET requiring the source and drain diffusion layer regions of the high and low impurity concentrations.

4. Brief Description of Drawings

Figs. 1(a) to (e) are cross sectional views sequentially showing a manufacturing process in one embodiment of the present invention, in each of which a

portion of a high voltage withstanding MOSFET is shown on the left and a portion of an MOSFET of a high processing speed and a high integration is shown on the right, respectively; Figs. 2(a) to (e) are cross sectional views sequentially showing manufacturing processes of a conventional high voltage withstanding MOSFET; Figs. 3(a) to (d) are cross sectional views sequentially showing a process in which two kinds of gate oxide films are formed on the same semiconductor substrate and which has already been filed; Fig. 4 is a concentration distribution graph of a high impurity concentration N type diffusion layer formed according to the embodiment of the present invention; and Fig 5 is a concentration distribution graph of a low impurity concentration N type diffusion layer.

1: P type silicon substrate, 2: gate oxide film of 1800 Å, 21: gate oxide film of 400 Å, 22: gate oxide film of 2000 Å, 3: gate electrode, 4: phosphorus ion, 6: source and drain diffusion layers of N type low impurity concentration, and 7: source and drain diffusion layers of N type high impurity concentration.

[Fig. 1]

1 ... Silicon substrate

2 ... Gate oxide film of 1800 Å

3 ... Gate electrode

6 ... Source and drain diffusion layers of low impurity concentration

7 ... Source and drain diffusion layers of high impurity concentration

21 ... Gate oxide film of 400 Å

22 ... Gate oxide film of 2000 Å

[Fig. 4] [Fig. 5]

a).. Impurity concentration

b).. Depth of diffusion

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㊹発明の名称 半導体集積回路の製造方法

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明細書

1.発明の名称 半導体集積回路の製造方法

2.特許請求の範囲

1)ソース・ドレイン拡散層領域がチャネル形成領域に近接した低不純物濃度領域とそれ以外の高不純物濃度領域とからなるMIS型FETを含む半導体集積回路の製造方法において、前記低不純物濃度拡散層領域と高不純物濃度拡散層領域を形成する際に、低不純物濃度拡散層を形成する領域上部のゲート絶縁膜厚を高不純物濃度拡散層を形成する領域上部のゲート絶縁膜厚と比較して厚くし、これらのゲート絶縁膜とゲート電極とをマスクにしてイオン注入を行うことを特徴とする半導体集積回路の製造方法。

3.発明の詳細な説明

〔産業上の利用分野〕

本発明は、ソース・ドレイン拡散層領域がチャネル形成領域に近接した低不純物濃度領域とそれ以外の高不純物濃度領域とからなるMIS型電界効果トランジスタ(FET)を含む半導体集積回路の製造方法に関する。

〔従来の技術〕

MIS型FETの高耐圧化を目的として、ソース・ドレイン拡散層領域のチャネル形成領域側端部に、同一の導電型で比較的低不純物濃度の拡散層領域を設けた構造が現在広く用いられている。第2図(a)～(e)にそのような構造のMOS型FETの製造方法におけるソース・ドレイン領域への不純物導入方法を示す。まずP型シリコン基板1上にゲート酸化膜2を介して形成された多結晶シリコンゲート電極3をマスクとして、1×10^{13}/cm²程度の低ドーズ量でりん4のイオン注入を行う(第2図(a))。次に、ゲート電極3およびソース・ドレイン拡散層において低不純物濃度領域とするべき領域をフォトレジスト膜5で覆った後(第2図(b))、今度は5×10^{15}/cm²程度の高ドーズ量で再びりんのイオン注入を行う(第2図(c))。次にフォトレジスト膜5を除去したのち(第2図(d))、熱処理を行うことにより、低不純物濃度および高不純物濃度のN型拡散領域6,7をもつ高耐圧構造

ＭＯＳ型ＦＥＴのソース・ドレイン拡散層領域を形成する（第２図(e)）。以上の工程によって形成されたソース・ドレイン低不純物濃度拡散層６を含むＭＯＳ型ＦＥＴを用いれば、通常のＭＯＳ型ＦＥＴと比較してドレイン拡散層での電界集中が緩和されるため、ソース・ドレイン間耐圧が向上する。

ところで、近年の半導体集積回路装置においては、上記のような高耐圧化を目的としたＭＩＳ型ＦＥＴと、高速，高集積化を目的とした微細なＭＩＳ型ＦＥＴとを同一の基板上に集積する技術が重要となっている。しかし、高速，高集積化を目的としたＦＥＴと高耐圧化を目的としたＦＥＴとを同一基板上に集積する場合、以下の問題点を克服する必要がある。すなわち、高速，高集積化を目的としたＦＥＴは比較的ゲート絶縁膜厚を薄くする必要があり、高耐圧化を目的としたＦＥＴは比較的厚くすることが必要である。ところが、従来の半導体装置においては、上記２種類のＦＥＴを同一のゲート導電膜上に作成していたため、高速，高集積化と高耐圧化を同時に満足することは極めて困難であった。そこで、この問題点を克服するための手段として、同一基板上に２種類以上の膜厚のゲート導電膜を備えた構造の半導体装置が本出願人の特許出願にかかる特願昭63－201473号明細書に記載されている。第３図(a)～(d)にこのような半導体装置におけるゲート酸化膜形成工程の一例を示し、以下にその工程を説明する。まず、通常の選択酸化法により素子領域以外のＰ型Si基板１上にフィールド酸化膜８を形成した後、素子領域に残された酸化膜を除去する（第３図(a)）。次いで乾燥酸素中の熱処理により、素子領域を含むウエハ全面に1800Åのゲート酸化膜２を形成する（第３図(b)）。次に、高耐圧Ｎチャネルｍｏｓ型ＦＥＴを形成する方の素子領域以外の部分をフォトレジスト膜５で覆った後、前記素子領域部分のゲート酸化膜２をふっ酸によるウェットエッチングにより除去する（第３図(c)）。その後、前記フォトレジスト膜５をO_2プラズマによるレジスト灰化により除去した後、乾燥酸素中の熱処理により今度は素子領域を含むウエハ全面に400Åの厚さのゲート酸化膜を形成する。以上の工程により高耐圧Ｎ型ＦＥＴの素子領域には2000Åの厚さのゲート酸化膜21，高集積，高速Ｎ型ＦＥＴの素子領域には400Åの厚さのゲート酸化膜22を得ることができる（第３図(d)）。

（発明が解決しようとする課題）

第２図および第３図に示した製造方法は、それぞれ高耐圧化を目的としたＭＩＳ型ＦＥＴと、高速，高集積化を目的としたＭＩＳ型ＦＥＴとを同一基板上に作成することに適した製造方法であり、両方の製造方法を組合わせることによって高耐圧ＭＩＳ型ＦＥＴと高速，高集積ＭＩＳ型ＦＥＴを同一基板上に作成でき、しかもゲート絶縁膜厚を高耐圧ＦＥＴでは厚くし、高速，高集積ＦＥＴでは薄くすることができる。ところが、これらの製造方法を単純に組合わせた場合、それぞれの目的に対応して追加された工程数は、単純に加算されることになり、従来の標準的なＭＩＳ型ＦＥＴの製造工程に比べ非常に多くなってしまうという欠点があった。

本発明の目的は、高耐圧ＭＩＳ型ＦＥＴが異なる種類のＭＩＳ型ＦＥＴと同一半導体基板に集積する場合でも工程数が少ない半導体集積回路の製造方法を提供することにある。

（課題を解決するための手段）

上記の目的の達成のために、本発明は、ソース・ドレイン拡散層領域がチャネル形成領域に近接した低不純物濃度領域とそれ以外の高不純物濃度領域とからなるＭＩＳ型ＦＥＴを含む半導体集積回路の製造方法において、前記低不純物濃度拡散層領域と高不純物濃度拡散層領域を形成する際に、低不純物濃度拡散層を形成する領域上部のゲート絶縁膜厚を高不純物濃度拡散層を形成する領域上部のゲート絶縁膜厚と比較して厚くし、これらのゲート絶縁膜とゲート電極とをマスクにしてイオン注入を行うものとする。

（作用）

ゲート絶縁膜の異なる領域上にイオン注入で不純物導入を行うことにより、一度だけのイオン注

入により2種類の不純物濃度をもった拡散層領域を形成することができ、これにより高耐圧化を目的としたＭＩＳ型ＦＥＴのソース・ドレイン拡散層の低不純物濃度領域および高不純物濃度領域が、例えば高速、高集積化を目的としたＭＩＳ型ＦＥＴのソース・ドレイン拡散層と同一工程で同一半導体基板に形成できるので、工程数を低減することができる。

（実施例）

第1図(a)～(e)は本発明の一実施例における製造工程を高耐圧ＭＯＳ型ＦＥＴの部分について各図の左側に、同一基板上の高速、高集積ＭＯＳ型ＦＥＴについて各図の右側にそれぞれ示したものであり、第2図、第3図と共通の部分には同一の符号が付されている。まず第3図に示した方法と同様に1000Åのゲート酸化膜2をＰ型Si基板上全面に形成し（第1図(a)）、その酸化膜の選択エッチングと乾燥酸素中の熱処理により2種類の膜厚のゲート酸化膜21,22を形成する（第1図(b)）。この際、高耐圧ＭＯＳ型ＦＥＴにおいては低不純物濃度拡散層を作成する領域上のゲート酸化膜22の厚さは2000Å、高不純物濃度拡散層を作成する領域上のゲート酸化膜21の厚さは400Åとする。また高速、高集積ＭＯＳ型ＦＥＴにおいては膜厚400Åのゲート酸化膜21を形成する。次に多結晶シリコンによってゲート電極3を形成したのち（第1図(c)）、ゲート電極3をマスクとして自己整合的にりん4のイオン注入を行う（第1図(d)）。このときのイオン注入条件は、P_{31}^{+}イオンを用いて加速電圧90keV、ドーズ量3.5×10^{13}／cm²である。この際Ｐ型シリコン基板に到達するP_{31}^{+}イオン4の量は、その基板表面にあるゲート酸化膜厚に依存し、ゲート酸化膜厚が厚いほどシリコン基板に到達するP_{31}^{+}イオンの量は少ない。従って窒素雰囲気中で熱処理を行い、P_{31}^{+}イオンを拡散・活性化してＮ型拡散層を形成した場合（第1図(e)）、膜厚2000Åのゲート酸化膜22の下の拡散層はＮ型低不純物濃度拡散層のソース・ドレイン領域6、膜厚400Åのゲート酸化膜21の下の拡散層は、Ｎ型高不純物濃度拡散層のソース・ドレイン領域7となる。上記拡散層の濃度分布を第4図、第5図に示す。第4図はＮ型高不純物濃度拡散層7の濃度分布、第5図はＮ型低不純物濃度拡散層6の濃度分布となっている。両図において線11がＮ型、線12がＰ型の濃度分布である。この図からわかるように、Ｎ型高不純物濃度拡散層7は高速、高集積ＦＥＴを駆動させるのに適した濃度分布となっており、またＮ型低不純物濃度拡散層6は高耐圧ＦＥＴにおいてドレイン部電界集中を緩和するのに十分な濃度分布となっている。

以上の方法によれば、ゲート酸化膜厚を2種類、同一基板上に作成する第3図に示した従来方法による製造工程を全く変えずに、ゲート酸化膜厚をエッチングにより2種類に分けるためのパターンの高耐圧ＭＯＳ型ＦＥＴにおけるソース・ドレイン部のみを変化させることによって、第2図に示したような高耐圧ＦＥＴを高速、高集積ＦＥＴと同一基板上に作成することができた。つまり第2図および第3図における従来方法を組合わせた場合と比較して、第2図における低不純物濃度拡散層形成工程、第2図(c)，(b)が省略できることになる。

（発明の効果）

本発明によれば、高耐圧ＭＩＳ型ＦＥＴと高速、高集積ＭＩＳ型ＦＥＴとの厚さの異なるゲート絶縁膜を同一基板上に形成する既出願の方法に基づく工程を利用し、高耐圧ＭＩＳ型ＦＥＴのソース・ドレイン部のゲート絶縁膜の膜厚を2種類に分けるためのパターンを用意するのみで、1回のイオン注入工程で高耐圧ＭＩＳ型ＦＥＴと、例えば高速、高集積ＭＩＳ型ＦＥＴとのソース・ドレイン部が同時に形成でき、高、低不純物濃度のソース・ドレイン拡散層領域を必要とする高耐圧ＭＩＳ型ＦＥＴを含む半導体集積回路の製造の際の工程数低減に極めて有効である。

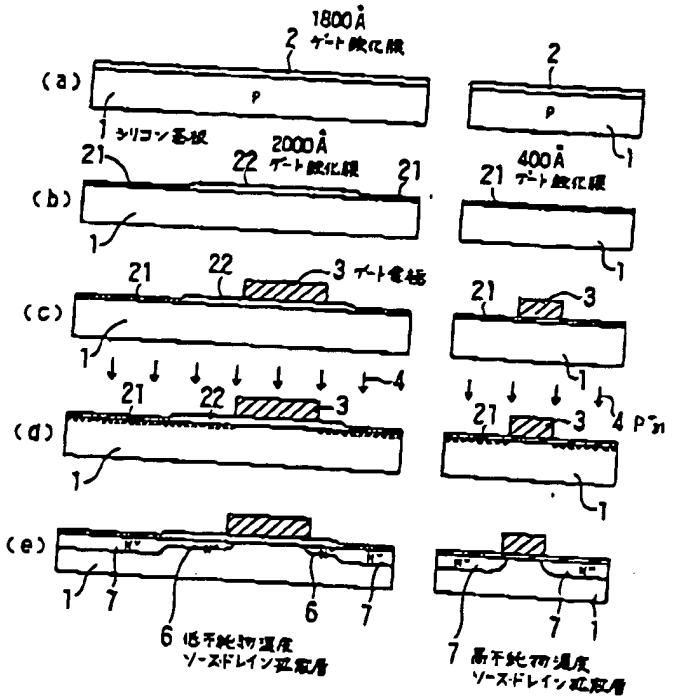
4.図面の簡単な説明

第1図(a)～(e)は本発明の一実施例における製造工程を高耐圧ＭＯＳ型ＦＥＴの部分についてる図の左側に、高速、高集積ＭＯＳ型ＦＥＴについて各図の右側にそれぞれ順次示した断面図、第2図

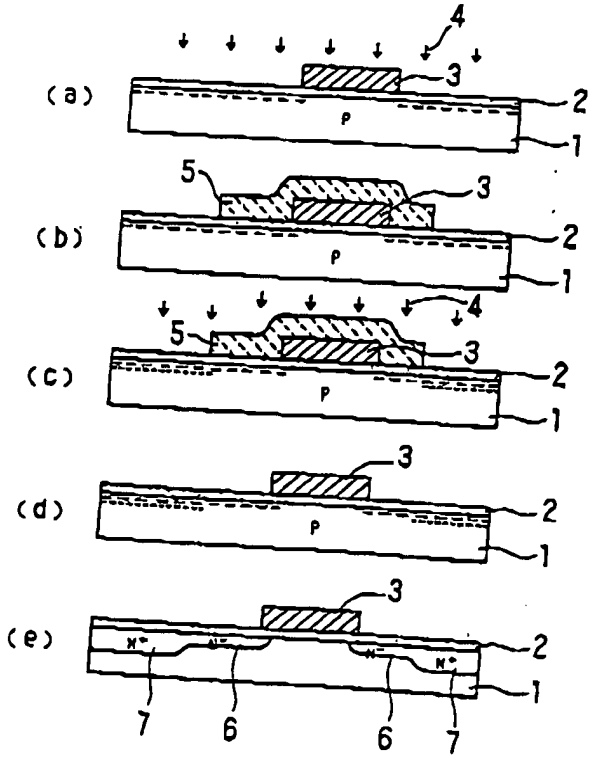
(a)～(e)は従来の高耐圧MOS型FETの製造工程を順次示す断面図、第3図(a)～(d)は同一半導体基板に2種類のゲート酸化膜を形成する既出願の工程を順次示す断面図、第4図は本発明の一実施例により形成された高不純物濃度N型拡散層の濃度分布図、第5図は同じく低不純物濃度N型拡散層の濃度分布図である。

1：P型シリコン基板、2：1800Åゲート酸化膜、21：400Åゲート酸化膜、22：2000Åゲート酸化膜、3：ゲート電極、4：りんイオン、6：N型低不純物濃度ソース・ドレイン拡散層、7：N型高不純物濃度ソース・ドレイン拡散層。

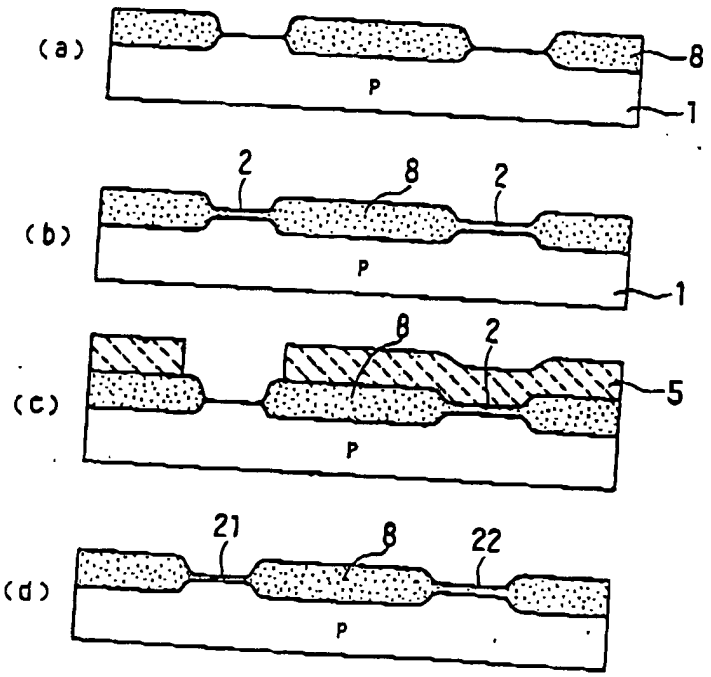
代理人弁理士 山口 巌



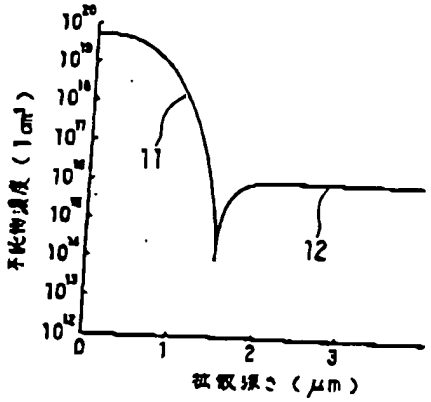
第1図



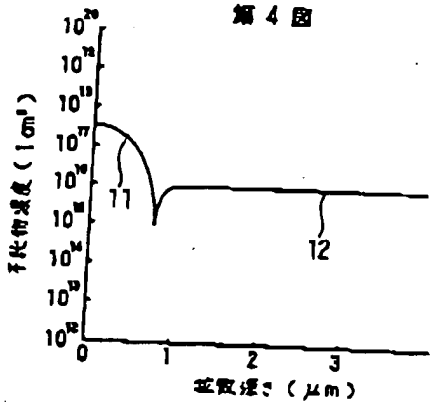
第2図



第3図



第4図



第5図